Amendments to the Drawings:

The attached sheet of drawing includes changes to Fig. 2A.

Attachment: Replacement Sheet
Annotated Sheet Showing Changes

REMARKS/ARGUMENTS

Claims 1-30 are pending in the present application.

This Amendment is in response to the Office Action mailed December 9, 2004. In the Office Action, the Examiner objected to the specification and the drawings, rejected claims 1-30 under 35 U.S.C. §103(a). Reconsideration in light of the remarks made herein is respectfully requested.

Drawings

1. The Examiner objected to the drawings due to minor informalities. In response, Applicants have amended the drawings accordingly. The data path 230 is re-numbered 220 and the data path 240 is included. Therefore, Applicants respectfully request the objection be withdrawn.

Specification

1. The Examiner objected to the specification due to minor informalities. In response, Applicants have amended the specification accordingly. Therefore, Applicants respectfully request the objection be withdrawn.

Claim Objections

1. The Examiner objects to claims 30 because of minor informalities. Applicants have amended claim 30 to correct the minor informalities. Applicant respectfully requests that the Examiner withdraw the objection to claims 30.

Rejection Under 35 U.S.C. § 103

1. In the Office Action, the Examiner rejected claims 1-30 under 35 U.S.C. §103(a). Applicants respectfully traverse the rejection and contend that the Examiner has not met the burden of establishing a prima facie case of obviousness. To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second,

there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *MPEP §2143, p. 2100-129 (8th Ed., Rev. 2, May 2004).* Applicants respectfully contend that there is no suggestion or motivation to combine their teachings, and thus no *prima facie* case of obviousness has been established.

Claims 1-2, 11-12, and 21-22 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 4,698,753 issued to Hubbins et al. ("Hubbins").

Hubbins discloses a multiprocessor interface device. The device has ports A and B connected respectively to the bus systems of processors A and B and the ports are connected to a multiplexer to a common memory (Hubbins, col. 3, lines 29-31). The device has mode pins to define 4 modes. In the master and slave mode, the devices may be employed in parallel to accommodate wider word length (Hubbins, col. 10, lines 5-23).

The Examiner states that Hubbins discloses a multiplexer coupled to the first and second processors and to a slave, in this case the memory (Office Action, page 4, item 7). Applicants respectfully disagree. First, as clearly shown in Figure 1 in Hubbins, the multiplexer is merely connected to ports A and B and a 256x8 RAM. Ports A and B are contained inside the device (Hubbins, col. 3, lines 60-65; Figure 2, elements 2, 3, and 1). Since the ports are inside the device, they cannot be master buses. A master bus should be outside of a device to provide interface access to a plurality of other processors. Second, there is no slave bus. The memory is connected directly to the multiplexer. Third, even if there is a slave bus connected to the memory, this bus is still inside the device and is not available for external connections. Fourth, there is no plurality of slave buses because there is only one memory connected internally to the multiplexer.

The Examiner further states that while Hubbins does not explicitly teach that there is a plurality of slave buses, he does teach that several devices can be used in parallel (Office Action, page 4, item 7). Applicants respectfully disagree. Using several devices in parallel does not mean that a plurality of slave buses exists. Arranging these devices in parallel merely expands the width of the word length, e.g., from D0 – D7 to D0 – D7, D8 – D15, and D16 – D23 (Hubbins, Figure 9).

Hubbins effectively teaches away from the invention because all the interface circuits are located internally to a device. There are no external interfaces for the memory other than through the two ports A and B. There are no first and second master buses and there cannot be a plurality of slave buses.

Claims 3, 13, and 23 is rejected under 35 U.S.C. §103(a) as being unpatentable over Hubbins as applied to claims 1-2 above, and further in view of U.S. Patent No. 5,590,369 issued to Burgess et al. ("Burgess").

Hubbins is discussed above.

Burgess discloses a bus supporting a plurality of data transfer sizes and protocols. A peripheral bus (Pbus) is used for transferring data between a processor and various peripheral devices (also denoted slaves) (Burgess, col. 4, lines 47-51). A Pbus master controls the operation of the Pbus (Burgess, col. 4, lines 52-54). The address bus connects the Pbus master with a synchronous/ asynchronous address decoder (Burgess, col. 6, lines 19-21). This decoder pairs each slave device with a corresponding address selected line connected to the slave(s) involved in the data transfer (Burgess, col. 6, lines 25-28).

Hubbins and Burgess, taken alone or in combination, do not disclose, suggest, or render obvious an address decoder coupled to the bus arbiter and the first mutiplexer to decode the slave address. As discussed above, Hubbins does not disclose a first multiplexer coupled to first and second master buses and slave address. Burgess merely discloses an address decoder to pair each slave device with a corresponding address selected line, not to decode a slave address in a plurality of slave buses.

Furthermore, if the proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. In re Gordon, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984). MPEP 2143.01. Here, Hubbins discloses a single memory inside a device. Modifying the device to include the address decoder to access multiple devices as provided by Burgess would render Hubbins device unsatisfactory because its intended purpose is to allow accessing to a single memory, not a plurality of memories (Hubbins, col. 3, lines 29-32).

Claims 4-5 and 7-10, 14-15 and 17-20, and 24-25 and 27-30 are rejected under 35 U.S.C. §103(a) as being unpatentable over Hubbins and Burgess as applied to claim 3 above, and further in view of U.S. Patent No. 5,453,737 issued to Opoczynski ("Opoczynski").

Hubbins and Burgess are discussed above.

Opoczynski discloses a control and communication apparatus. A master controller communicates with a plurality of slave subsystems (Opoczynski, col. 2, lines 25-27). A serial port is connected through a selector, which receives a select line from the controller processor and controls which of the line drivers/receivers circuits receive the serial port I/O stream (Opoczynski, col. 3, lines 65-67; col. 4, line 1).

Hubbins, Burgess, and Opoczynski, taken alone or in any combination, do not disclose, suggest, or render obvious (1) a second multiplexer coupled to the first slave bus to provide bus response information from device response information using the device select signal; and (2) a de-multiplexer coupled to the second multiplexer and the first and second master buses to transfer the bus response information to one of the first and second processors using the arbitration select signal. As discussed above, Hubbins does not disclose a first multiplexer coupled to first and second master buses and slave address. Burgess does not disclose an address decoder to decode slave address. Opoczynski merely discloses a selector to control which of the line drivers/receivers receives the serial port I/O stream. The serial port I/O stream is not the same as the bus response information from device response information. Furthermore, the selector is not connected to a first slave bus that is also connected to another multiplexer.

The Examiner states that multiplexer 21 of Figure 2 of Hubbins is bi-directional to allow for reads and writes to memory, so it performs the functions of a multiplexer and de-multiplexer (Office Action, Page 5, item 10). Applicants respectfully disagree. The multiplexer 21 is connected at the output of the memory to the data registers (Hubbins, col. 4, lines 36-38). A multiplexer can only be used in one direction. It cannot function as both a multiplexer and a demultiplexer. Furthermore, the multiplexer 21 does not provide the bus response information and transfer it to one of the two processors.

Claims 6, 16, and 26 are rejected under 35 U.S.C. §103(a) as being unpatentable over Hubbins, Burgess and Opoczynski as applied to claim 4-5 and 7-10 above, and further in view of U.S. Patent No. 5,717,8957 issued to Leedom et al. ("Leedom").

Leedom discloses an associative scalar data cache with write-through capabilities for a vector processor. A scalar/vector supercomputer includes a scalar/vector processor connected through a common memory interface to one or more sections of common memories (Leedom, col. 5, lines 19-23).

Hubbins, Burgess, Opoczynski, and Leedom, taken alone or in any combination, do not disclose, suggest, or render obvious the plurality of slave buses being coupled to a common memory via a common memory interface. As discussed above, Hubbins, Burgess, and Opoczynski, individually or collectively, do not disclose first and second master buses, a plurality of slave buses, a multiplexer, an address decoder, a second multiplexer, and a de-multiplexer. Leedom merely discloses a common memory interface to a scalar/ vector processor. A scalar/ vector processor is not a slave device connected to a slave bus. The common memory interface in Leedom is connected directly to the V registers, the B and T registers, the address selector, and the instruction buffers (Leedom, Figure 1), not to a plurality of slave buses.

Therefore, Applicants believe that independent claims 1, 11, 21 and their respective dependent claims are distinguishable over the cited prior art references. Accordingly, Applicants respectfully request the rejections under 35 U.S.C. §103(a) be withdrawn.

Conclusion

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: March 7, 2005 By_____

Thinh V. Nguyen
Reg. No. 42,034
Tel.: (714) 557-3800 (Pacific Coast)

Attachments

12400 Wilshire Boulevard, Seventh Floor
Los Angeles, California 90025

CERTIFICATE OF MAILING/TRANSMISSION (37 CFR 1.8A)

I hereby certify that this correspondence is, on the date shown below, being:

MAILING

☒ *deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450.*

Date: 03/07/2005

FACSIMILE

☐ *transmitted by facsimile to the Patent and Trademark Office.*

03/07/2005

Tu Nguyen *Date*

Annotated Sheet Showing Changes

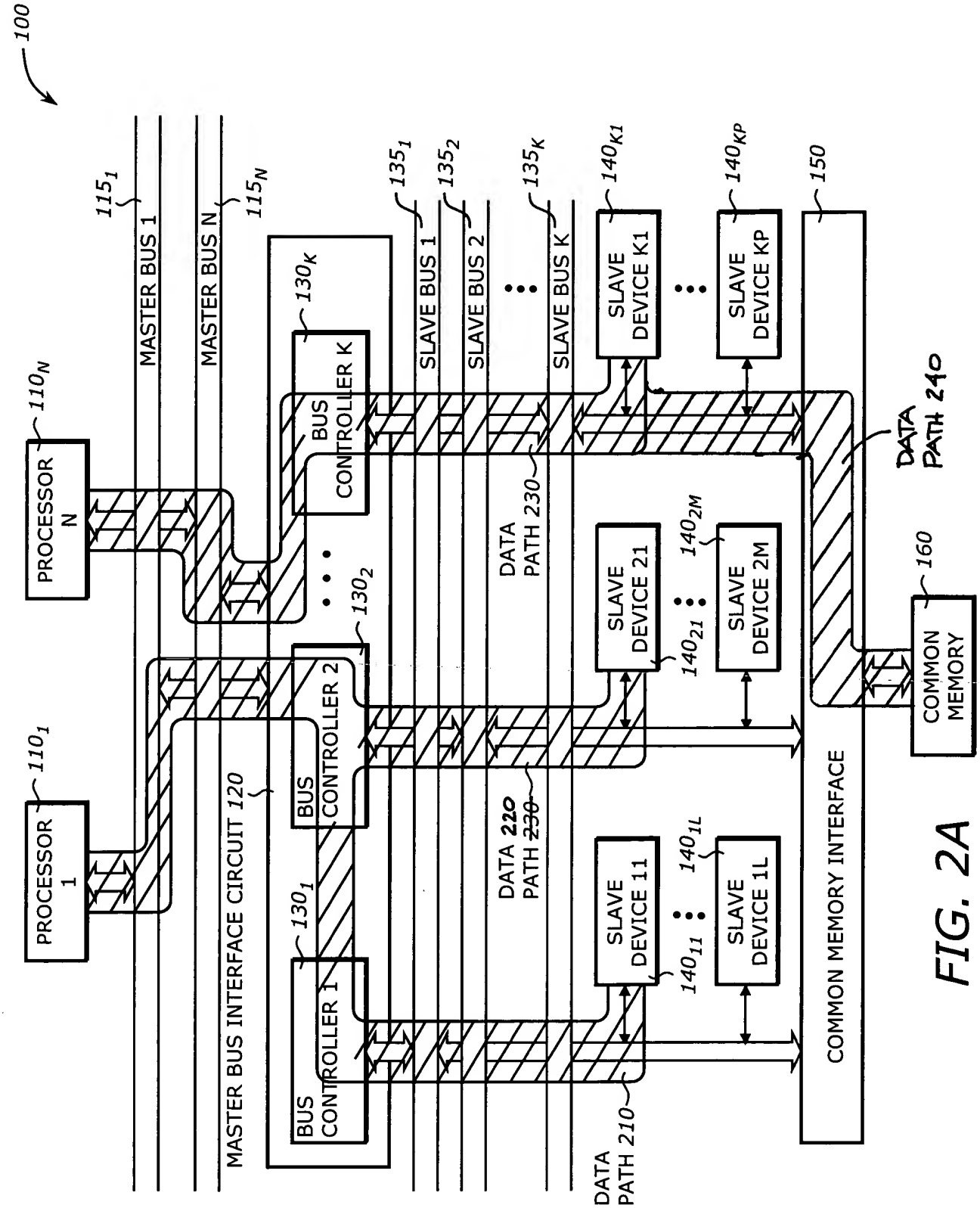

FIG. 2A